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In-Process DPMO and Estimated Yield for PWAs

Developed by the DPMO and Assemblies, Attributes and Variables Identification Task Group (5-22g) of the Assembly and Joining Processes Committee (5-20) of IPC

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Users of this standard are encouraged to participate in the development of future revisions.

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1 OVERVIEW

1.1 Scope This document defines standard methodologies for calculating defects per million opportunities (DPMO) metrics related to electronic printed board assembly processes. It is intended for use in measuring in-process assembly steps rather than end product determination. Calculation of completed item DPMO is addressed in IPC-7912.

Additionally, a guide to defect categorization is provided that when used with IPC/EIA J-STD-001 and IPC-A-610 can serve as a base for summarizing and reporting in-process defects.

Note: This document does not dictate the number of assemblies or data points needed to calculate DPMO metrics.

1.2 Purpose The purpose of this document is to define consistent methodologies for computation of **in-process** DPMO metrics for any defect evaluation stage in the assembly process.

This objective anticipates the following conditions in defect reporting and analysis:

- To facilitate process improvement, defects discovered at any stated inspection or test point should be assigned to their appropriate process step.
- All defects shall be reported at the inspection point they are found, even though one undetected previous defect may have caused the subsequent defects.
- Regardless of how these defects are assigned, the defect must be attributed to either a component, placement, termination or assembly defect.
- The assumption is that each printed board assembly that is inspected will be 100% inspected for all defects.
- The assumption of 100% inspection efficiency is made. Care should be exercised when comparing processes using manual inspection to those using automated vision inspection.
- When using a sampling inspection plan, the number of PWAs **inspected** determines the opportunity count, not the number **processed**.

1.3 Terms and Definitions

DPMO (Defects per Million Opportunities) is defined as the total number of defects divided by the total number of opportunities for a defect multiplied by 1,000,000. It is not strictly equivalent to ''PPM'' as the definition of ''opportunities'' has special meaning when considering electronic assembly processes.

DPU (Defects per Unit) is defined as the average number of defects per PWA.

Process Step Estimated Yield The expected percentage of assemblies with no defects for a particular process step or combined process steps, based on historical defect rates.

Component Opportunities (o_c) The term ''component'' is defined as each device or piece of hardware that may be assembled onto a printed wire board (PWB). Solder, glue dots, and other similar materials are not to be included in this DPMO calculation. The PWB is considered to be one component.

The total opportunity count for each ''component'' is one. An electronic component with multiple leads still counts as one. Processes, such as conformal coating and cleaning operations, do not add component opportunity counts. These are captured in one assembly opportunity. The finished PWA is not an opportunity.

Component Defect (d_c) A component defect is damage to a component exceeding the limits of the component specification, or those described in J-STD-001, and/or damage that results in non-usability of that component. Component defects include both visible and non-visible defects (physical/electrical). *Example:* A component could be both dimensionally incorrect and have major surface flaws, however, this results in a defect count of one.

Placement Opportunity (o_p) The term ''placement'' refers to the presence and/or positioning of any component on a PWB. The PWB does not have a placement opportunity, therefore the number of placements is one less than the number of components. This is because the printed wiring board has no ''placement'' of its own. The total opportunity count for each placed component is one.

Placement Defect (d_p) A placement defect is any component presence and/or positioning error that has occurred during an assembly operation that violates the dimensional criteria specified for that component in IPC/EIA J-STD-001 or IPC-A-610. Example: Exceeding maximum side or toe overhang. Even though a component may have more than one placement defect, any one or combination of multiple placement defects on any single component has a maximum defect count of one for that placement.

Termination Opportunity (o_t) The term ''termination'' is defined as any hole, land or other surface (such as component to component attachment) to which a component may be electrically terminated. This includes any terminal onto which a wire is electrically attached.