ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES ®

IPC-9151

Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database

IPC-9151
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A standard developed by IPC

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Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database

Developed by the PCQR^2 Subcommittee (D-36) of the Rigid Printed Board Committee (D-30) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC PCQR^2 Subcommittee (D-36) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Printed Board Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database

1 SCOPE

1.1 Purpose The purpose of this document is to define a Process Capability, Quality, and Relative Reliability (PCQR^2) Benchmark Test Standard and Database subscription system, for the evaluation of printed wiring board manufacturing processes and the mechanism that allows the comparative data to be accessible industry wide. This is in accordance with The National Technology Roadmap for Electronic Interconnections 2000/2001 published by IPC, which states that "For a company to efficiently manage its supply chain it must identify the capability of its suppliers and make certain that their capability for manufacturing a product is consistent with the needs of the customer."

1.2 Documentation Hierarchy All other IPC documents take precedence over this document. This document describes a process to evaluate the manufacturing capability of key attributes specified in the design and acceptability standards controlled by IPC.

1.3 Definition of Terms

1.3.1 Conductor Analysis Technologies Inc. (CAT Inc.) A New Mexico-based Company providing and controlling the intellectual property associated with the PCQR^2 process capability panels, data analysis techniques, and database.

1.3.2 Printed Wiring Board Fabricator A company or organization that manufactures printed wiring boards.

1.3.3 Manufacturing Facility The physical site of a company or organization that fabricates the process capability panels.

1.3.4 Process Capability Panel A parametric test panel that is comprised of test modules designed to evaluate specific characteristics of printed wiring board manufacturing processes.

1.3.5 Test Module The individual element of a process capability panel.

1.3.6 Design Library The family of available process capability panel designs developed by the D-36 Subcommittee.

1.3.7 Design Documentation File The file used to detail the manufacturing requirements and specification of each process capability panel design.

1.3.8 CAT Analysis Report Detailed data on each printed wiring board fabricator's process capability and quality.

1.3.9 Process Capability Data The data generated from the testing of PCQR^2 process capability panels.

1.3.10 PCQR^2 Database The electronic storage medium for the data and reports generated from the testing of PCQR^2 process capability panels.

1.3.11 Valid Data Current entries in the "Industry Statistics" and "Process Capability Data" databases, the latter of which is only accessible to subscribers and remains available for review and comparison for twenty-four months from the posting date. The "Industry Statistics" database will encompass data from all submittals regardless of posting date.

1.3.12 Process Capability Report Comparative data of each printed wiring board fabricator participating in the PCQR^2 database.

1.3.13 Industry Statistics Statistical data on the industry's capability and quality.

1.3.14 Annual Subscription License The method used by subscribers to gain access to the PCQR^2 Database.

1.3.15 Subscription Fee The fee paid by subscribers to access the PCQR^2 Database.

1.3.16 Supplier Information Form The form filled out by PCB suppliers upon submitting panels to the database, with pertinent information including board fabrication company and facility, contacts, via structures, fabrication materials, and stackup.

1.4 Applicable Documents[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

1. www.ipc.org

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC 9501 PWB Assembly Process Simulation for Evaluation of Electronic Components

IPC 9504 Assembly Process Simulation for Evaluation of Non-IC Components (Preconditioning of Non-IC Components)

2 PROCESS SUMMARY

2.1 Introduction Many printed wiring board users have developed internal processes to evaluate the capabilities of their printed wiring board fabricators. Fabricators often receive multiple requests from multiple customers to manufacture test panels as part of qualification procedures. The PCQR^2 process provides an industry standard for the design of these test panels. The resulting data provides the user (subscriber) with the ability to review detailed results from individual fabricators, and to compare the capabilities of multiple fabricators.

2.2 Process Steps

- At the request of a subscriber or on their own behalf, a printed wiring board fabricator may download the appropriate process capability panel design from the PCQR^2 design library at www.pcbquality.com.
- The fabricator manufactures the design using standard processes, and per the requirements and specifications outlined in the design documentation file and Section 6.
- CAT Inc. performs the required testing and analysis of the process capability panels.
- Reports and summary information are posted anonymously to the database and remain available for twenty-four months from the posting date.
- The fabricator is provided with their report and granted access to comparative statistics for a period of twelve months from the posting date.
- Subscribers are informed of the posting, and the requestor is informed of the fabricator's identity.
- Subscribers may request the identity of fabricators, but the fabricator must initiate the contact and identification.

3 UPDATES AND REVISIONS

3.1 Designs and Database The design library and database will be reviewed and updated periodically using the IPC subcommittee structure. Additions, deletions, and modifications will be made to the design library and database to reflect the needs of the subscribers and suppliers. These revisions will be coordinated through the PCQR^2 forum (pcqr2@ipc.org) and must be approved by the active subscribers and suppliers. In all cases, the most current revisions will be posted at www.pcbquality.com and are the controlling design documents. The most current designs shall be used; requests to support archived designs more than six months old will not be accepted.

3.2 Anonymity To maintain the anonymity of fabricators participating in the database, the subcommittee will refrain from discussions of specific fabricator identities and capabilities. The subcommittee will as necessary take appropriate steps to ensure this anonymity.

4 PROCESS CAPABILITY PANELS

4.1 Panel Layouts The process capability panels consist of an array of 25.4 mm x 25.4 mm [1.0 in x 1.0 in] test modules, and a 25.4 mm [1.0 in] border that includes nomenclature and alignment features (see Figures 4-1 and 4-2). Individual design layout maps can be found in the design documentation files posted at the www.pcbquality.com. The test module types include conductor and space, via registration, controlled-depth-drill overshoot, via daisy chain, soldermask registration, and controlled impedance.

4.2 Test Modules The test modules are designed to collect detailed information on a range of feature types and sizes. Table 4-1 details the information that is obtained from each of the modules.

4.3 Via Structures There is a variety of via structures included within each of the process capability panel designs. These structures are outlined in Table 4-2 and an example is depicted in Figure 4-3.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
P																							P
O																							O
N																							N
M																							M
L																							L
K																							K
J																							J
I																							I
H																							H
G																							G
F																							F
E																							E
D																							D
C																							C
B																							B
A																							A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

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Figure 4-1 457.2 mm x 609.6 mm [18 in x 24 in] Process Capability Panel Layout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
J																	J
I																	I
H																	H
G																	G
F																	F
E																	E
D																	D
C																	C
B																	B
A																	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

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Figure 4-2 304.8 mm x 457.2 mm [12 in x 18 in] Process Capability Panel Layout

Table 4-1 Test Module Statistical Attributes

Test Module	Capability Information	Quality Information
Conductor/Space	Conductor and space defect density	Conductor width and height uniformity
Via Registration	Via probability of breakout	
Drill Overshoot	Probability of overshoot	
Via	Via defect density	Via net resistance coefficient of variation
Via (Reliability)	Yield loss	Percent change in resistance
Soldermask Registration	Clearance yield	
Controlled Impedance	Impedance uniformity	

Table 4-2 Via Module Structures
(Note: Only the through-vias must be fabricated; fabrication of blind and buried via holes is optional)

Layer Count	Thickness	Through	1-Deep Blind	2-Deep Blind	3-Deep CDD	Buried Core
6	0.787 mm [0.031 in]	X	X	X		
	1.575 mm [0.062 in]					
12	1.575 mm [0.062 in]	X	X	X		X
18	2.362 mm [0.093 in]	X	X	X	X	X
24	3.175 mm [0.125 in]	X	X	X	X	X
	6.350 mm [0.250 in]	X				X

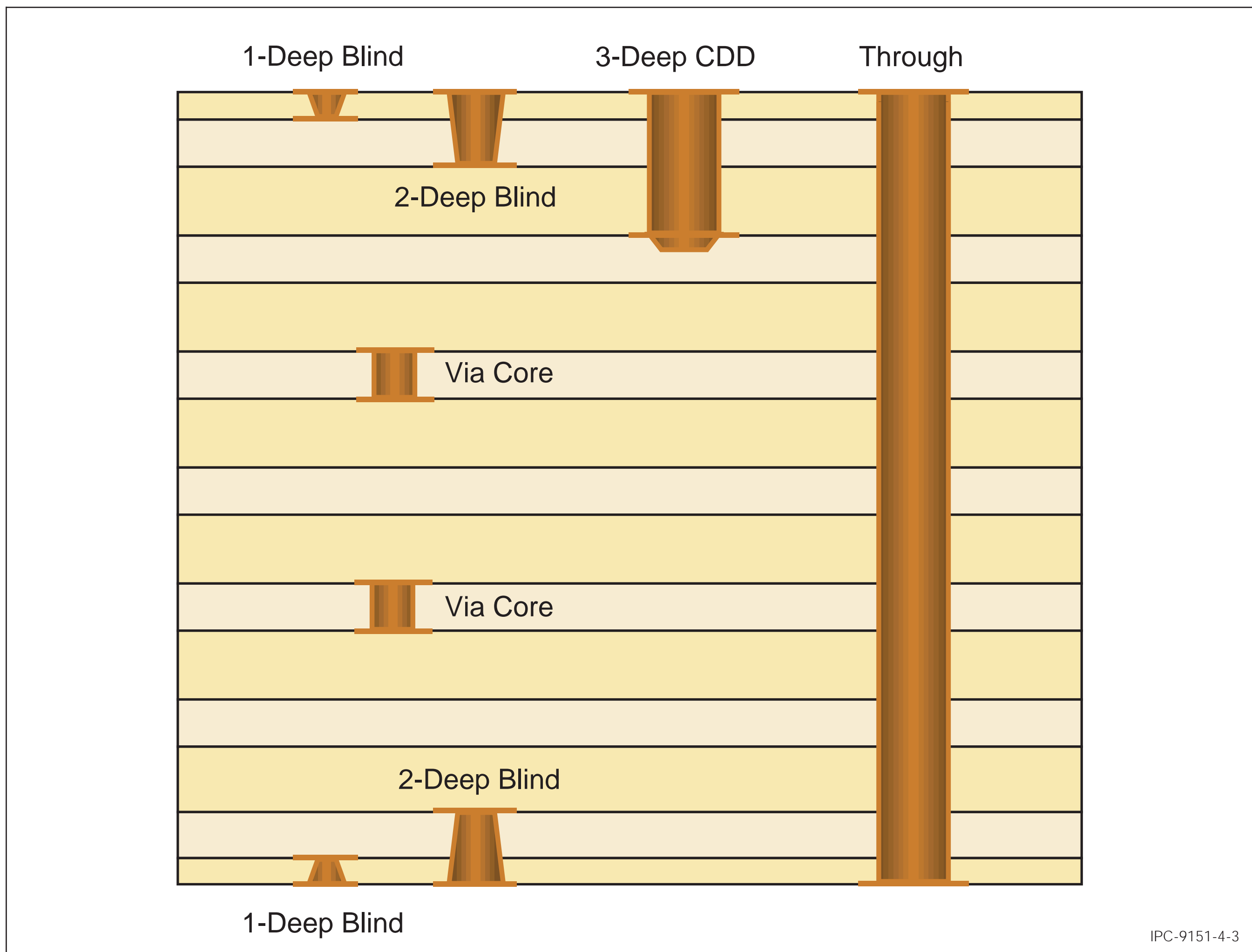

Figure 4-3 18-Layer Test Module Via Structures

5 DESIGN LIBRARY

The process capability panel design library is detailed in Table 5-1. Each of the designs has an accompanying documentation file that describes its specific features and manufacturing requirements. Tables 5-2 through 5-10 detail the feature types and sizes included in each of the designs, and show the difference between 'medium' and 'high' technology.

Table 5-1 Design Library
(Note: The most current design library is available at www.pcbquality.com)

Layer Count	Thickness	Panel Size	Technology	Design
6	0.787 mm [0.031 in]	304.8 mm x 457.2 mm [12 in x 18 in]	Medium	IPC-001A
			High	IPC-002A
		457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-003A
			High	IPC-004A
	1.575 mm [0.062 in]	304.8 mm x 457.2 mm [12 in x 18 in]	Medium	IPC-005A
			High	IPC-006A
		457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-007A
			High	IPC-008A
12	1.575 mm [0.062 in]	457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-009A
			High	IPC-010A
18	2.362 mm [0.093 in]	457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-011A
			High	IPC-012A
24	3.175 mm [0.125 in]	457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-013A
			High	IPC-014A
	6.350 mm [0.250 in]	457.2 mm x 609.6 mm [18 in x 24 in]	Medium	IPC-015A
			High	IPC-016A

Table 5-2 Outerlayer Conductor and Space Features

	0.787 mm [0.031 in]		1.575 mm [0.062 in]		2.362 mm [0.093 in]		3.175 mm [0.125 in]		6.350 mm [0.250 in]	
Design	H	M	H	M	H	M	H	M	H	M
Conductor Width (mils)	2									
	3		3		3		3			
	4	4	4		4		4		4	
	5	5	5	5	5	5	5	5	5	
		6	6	6	6	6	6	6	6	6
		7		7		7		7	7	7
				8		8		8		8
										9
Space Width (mils)	3		3							
	4		4		4					
	5	5	5	5	5		5			
		6		6	6	6	6		6	
		7		7		7	7	7	7	
						8		8	8	8
								9		9
										10

Table 5-3 Innerlayer Conductor and Space Widths

Design	0.5 oz		1.0 oz		Buried Core	
	H	M	H	M	H	M
Conductor Width (mils)	2					
	3		3		3	
	4	4	4		4	
	5	5	5	5	5	5
		6	6	6	6	6
		7		7		7
				8		8
Space Width (mils)	3					
	4		4		4	
	5	5	5		5	
		6	6	6	6	6
		7		7		7
				8		8

Table 5-4 Via Registration Designed Clearances
(Note: CDD=Controlled Depth Drill)

Design	Through					Blind		3-Deep CDD
	0.787 mm [0.031 in]	1.575 mm [0.062 in]	2.362 mm [0.093 in]	3.175 mm [0.125 in]	6.350 mm [0.250 in]	1-Deep	2-Deep	
Annular Ring (mils)						1	1	
	2					2	2	
	3	3				3	3	3
	4	4	4	4	4	4	4	4
	5	5	5	5	5	5	5	5
	6	6	6	6	6	6	6	6
	7	7	7	7	7			7
		8	8	8	8			8
			9	9	9			

Table 5-5 Controlled Depth Drill Overshoot Drill Sizes

Design	High	Medium
Drill Diameter (mils)	14.0	
	16.0	
	18.0	18.0
	20.0	20.0
		22.5
		25.0

Table 5-6 Via Structures and Associated Layers
(Note: Only the through-vias must be fabricated; fabrication of blind and buried via holes is optional)

Layer Count	Thickness	Through	1-Deep Blind	2-Deep Blind	3-Deep CDD	Buried Core
6	0.031	1-6	1-2, 6-5	1-3, 6-4		
	0.062	1-6	1-2, 6-5	1-3, 6-4		
12	0.062	1-12	1-2, 12-11	1-3, 12-10		4-5, 8-9
18	0.093	1-18	1-2, 18-17	1-3, 18-16	1-4	6-7, 12-13
24	0.125	1-24	1-2, 24-23	1-3, 24-22	1-4	6-7, 18-19
	0.250	1-24				6-7, 18-19

Table 5-7 Through Via Design Features
(Note: All via pads are tear-dropped)

Design	0.787 mm [0.031 in]		1.575 mm [0.062 in]		2.362 mm [0.093 in]		3.175 mm [0.125 in]		6.350 mm [0.250 in]	
	H	M	H	M	H	M	H	M	H	M
Drill Size (mils)	6									
	8		8		8					
	10	10	10		10		10			
	12	12	12	12	12	12	12			
		13.5	13.5	13.5	13.5	13.5	13.5	13.5		
		14.5		14.5		14.5	14.5	14.5		
				16		16		16	16	
								18	18	
									20	20
									22.5	22.5
										25
										28
Annular Ring (mils)	5	5	5	5	5	5	5	5	6	6
Track Width (mils)	10	10	10	10	10	10	10	10	10	10
Grid (mils)	40	40	40	40	40	40	40	40	52	52

Table 5-8 Blind and Buried Via Features
(Note: All via pads are tear-dropped)

Design	1-Deep Blind		2-Deep Blind		3-Deep CDD		Buried Core	
	H	M	H	M	H	M	H	M
Drill Size (mils)	3						3	
	4						4	
	5	5					5	5
	6	6					6	6
		7	7					7
		8	8					8
			9	9				
			10	10				
				11				
				12				
					14			
					16			
					18	18		
					20	20		
						22.5		
						25		
Annular Ring (mils)	4	4	4	4	5	5	4	4
Track Width (mils)	6	6	6	6	10	10	6	6
Grid (mils)	28	28	32	32	47	47	28	28

Table 5-9 Soldermask Registration Designed Clearances

Design	High	Medium
Clearance (mils)	1.0	1.0
	1.5	1.5
	2.0	2.0
	2.5	2.5
	3.0	3.0
	3.5	3.5

Table 5-10 Impedance Structures
(Note: Edge-Coupled Differential Striplines are on a 15-mil pitch)

	6-Layer		12-Layer	18-Layer	24-Layer	
Design	0.787 mm [0.031 in]	1.575 mm [0.062 in]	1.575 mm [0.062 in]	2.362 mm [0.093 in]	3.175 mm [0.125 in]	6.350 mm [0.250 in]
18-mil Surface Microstrip		X				
5-mil Surface Microstrip	X	X	X	X	X	X
18-mil Embedded Microstrip		X				
5-mil Embedded Microstrip	X	X	X	X	X	X
5-mil Symmetric Stripline				X	X	X
5-mil Offset Stripline	X	X	X		X	X
5-mil Offset Stripline (via core)				X	X	X
5-mil Edge-Coupled Differential Symmetric Stripline				X	X	X
5-mil Edge-Coupled Differential Offset Stripline					X	X
5-mil Edge-Coupled Differential Offset Stripline (via core)			X	X	X	X
5-mil Broadside-Coupled Differential Stripline					X	X
5-mil Broadside-Coupled Differential Stripline (via core)			X	X	X	X

6 GENERAL MANUFACTURING REQUIREMENTS AND SPECIFICATIONS

The design documentation file details the manufacturing requirements and specifications of each process capability panel design. The general manufacturing requirements and specification for the designs are as follows:

- A minimum of 30 panels (60 for the 457.2 mm x 609.6 mm [12 in x 18 in] designs) is required to obtain statistically valid data.
- No drawing is provided - build per Gerber data and the instructions in the design documentation file.
- The panels must be fabricated by the manufacturing facility being evaluated using standard production processes.
- The panels are to be manufactured in at least three lots, with a minimum of one week between the start of each lot.
- Tool the design as a new production part. A test lot for dimensional scaling and impedance verification is allowed.
- Copper filler patterns may be added to both the outerlayers and innerlayers, with the exception of the impedance modules.
- The panel borders may be used for tooling, but leave as much of the original border intact as possible.
- Do not obliterate the registration targets located in the borders of each panel side.
- Do not make repairs (welds or cuts) to opens or shorts (defects are expected).
- All pad surfaces must be clean for accurate test results to be obtained. Oxides or other contamination on pad surfaces will compromise test results.

7 TESTING AND ANALYSIS

7.1 Submission Rules At the request of a database subscriber(s) or on their own behalf, printed wiring board fabricators may download the appropriate process capability panel design(s) from the design library. Printed wiring

board fabrications may submit multiple sets of panels for each design. The manufacturing requirements and specification for each design are outlined in the design documentation files.

7.2 Build Time An embedded "date code" is included in the Gerber data, and is updated weekly to reflect the approximate fabrication starting time. When the panels are submitted for testing and analysis, the fabrication time is calculated from the "date code" and the submission date. The target delivery time for the designs is shown in Table 7-1.

Table 7-1 Target Delivery Time

Layer Count	Technology	Target Delivery Time (weeks)
6	Medium	6
	High	8
12	Medium	8
	High	10
18	Medium	12
	High	14
24	Medium	14
	High	16

7.3 Electrical Test and Data Analysis The panels will be tested and analyzed by Conductor Analysis Technologies, Inc. or by a third-party licensed by Conductor Analysis Technologies, Inc., and approved by the $PCQR^2$ Subcommittee. The typical testing, analysis and posting of data will be completed three weeks after receipt of all lots of panels and the Supplier Information Form. The type of test performed on each module is detailed in Table 7-2.

Table 7-2 Electrical Tests

Test Type	Test Module
Precision Resistance	Conductor/Space
	Via
	Via (Reliability)
Resistance	Via Registration
	Drill Overshoot
	Soldermask Registration
Time Domain Reflectometry (TDR)	Controlled Impedance

7.4 Assembly Simulation Six panels from each set of 30 will be subjected to six cycles of a tin/lead assembly simulation (convection reflow process) by CAT Inc. The panels are to be flipped after each cycle. The panels will not be conditioned by drying in an oven to remove moisture prior to assembly simulation. The thermal profile for the assembly simulation is detailed in Table 7-3. The cool down time is dependent on the panel thickness.

Table 7-3 Assembly Simulation Thermal Profile

Attribute	Heat-Up	Dwell	Cool-Down
Time (min.)	2	1	3-7
Temperature (°C)	25-183	183-215	25

7.5 Process Capability Panels Ownership The process capability panels are the property of the fabricator, and if requested will be returned to the fabricator once the testing and analysis has been completed. The panels will be stored for a period of three months from the posting of the data at which time CAT Inc. will dispose of the panels.

8 DATABASE

Data from process capability panel submissions is compiled into a database that details the process capability, quality, and relative reliability demonstrated by printed wiring board fabricators. The data remains active for a period of twenty-four months from the posting date. Printed wiring board fabricators may submit multiple sets of panels for each design.

8.1 Database Access Access to the database is provided through an annual subscription from IPC. Contact IPC or visit www.pcbquality.com for the subscription form and fee schedule. The subscription fee is based on the subscribers' annual corporate sales. Subscribers will have access to all sections of the database for evaluation purposes. Additionally, printed wiring board fabricators who submit panels to the database receive access to comparative industry statistics for a period of twelve months following the posting of their data.

8.2 Supplier Identity Request Subscribers to the database will be allowed to request the identity of the printed wiring board fabricators who have submitted panels to the database. Figure 8-1 details the supplier identity request process.

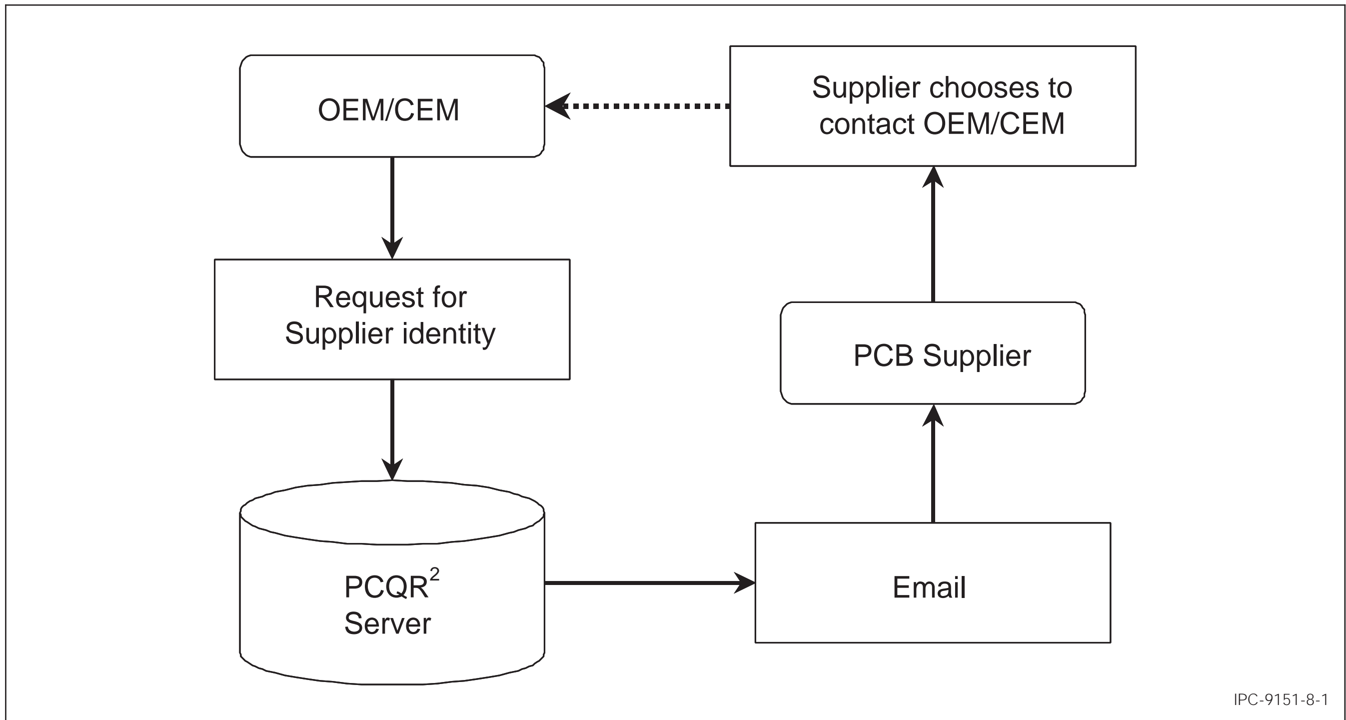

Figure 8-1 Supplier Identity Request

ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847 509.9798

SUBMITTOR INFORMATION:

Name: ____________________

Company: ____________________

City: ____________________

State/Zip: ____________________

Telephone: ____________________

Date: ____________________

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: ____________________

Document(s) to which this term applies: ____________________

Committees affected by this term: ____________________

Office Use

IPC Office	**Committee 2-30**
Date Received: ________	Date of Initial Review: ________
Comments Collated: ________	Comment Resolution: ________
Returned for Action: ________	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: ________	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:

Committee 2-30 has approved the above term for release in the next revision.

Name: ____________________ Committee: IPC 2-30 Date: ____________

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

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fax 847/509-9798
e-mail: answers@ipc.org

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TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, and job opportunities. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

Gencam@ipc.org

Gencam deals with issues regarding the Gencam™ standards and specifications for Printed Circuit Board Layout and Design.

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Message: <your message>

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For more information, contact Keach Sasamori
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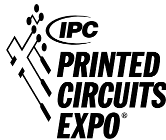

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tel 847/790-5386	tel 847/790-5398	e-mail: registration@ipc.org
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e-mail: MaryMacKinnon@ipc.org	e-mail: goapex@ipc.org

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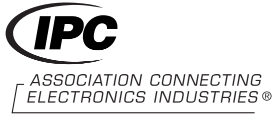

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To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category. *(Check one box only.)*

☐ Independent Printed Board Manufacturers

This facility manufactures and sells to other companies, printed wiring boards (PWBs) or other electronic interconnection products on the merchant market. What products do you make for sale?

☐ One-sided and two-sided rigid printed boards
☐ Multilayer printed boards
☐ Flexible printed boards
☐ Other interconnections

Name of Chief Executive Officer/President______________________________

☐ Independent Electronic Assembly EMSI Companies

This facility assembles printed wiring boards, on a contract basis, and may offer other electronic interconnection products for sale.

Name of Chief Executive Officer/President______________________________

☐ OEM–Manufacturers of any end product using PCB/PCAs or Captive Manufacturers of PCBs/PCAs

This facility purchases, uses and/or manufactures printed wiring boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line? ______________________________

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What products do you supply?______________________________

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02/01

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Standard Improvement Form

IPC-9151

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

   ___ Requirement, paragraph number __________

   ___ Test Method number __________, paragraph number __________

   The referenced paragraph number has proven to be:

   ___ Unclear ___ Too Rigid ___ In Error

   ___ Other ______________________________

2. Recommendations for correction:

   ____

   ____

   ____

   ____

3. Other suggestions for document improvement:

   ____

   ____

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