



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

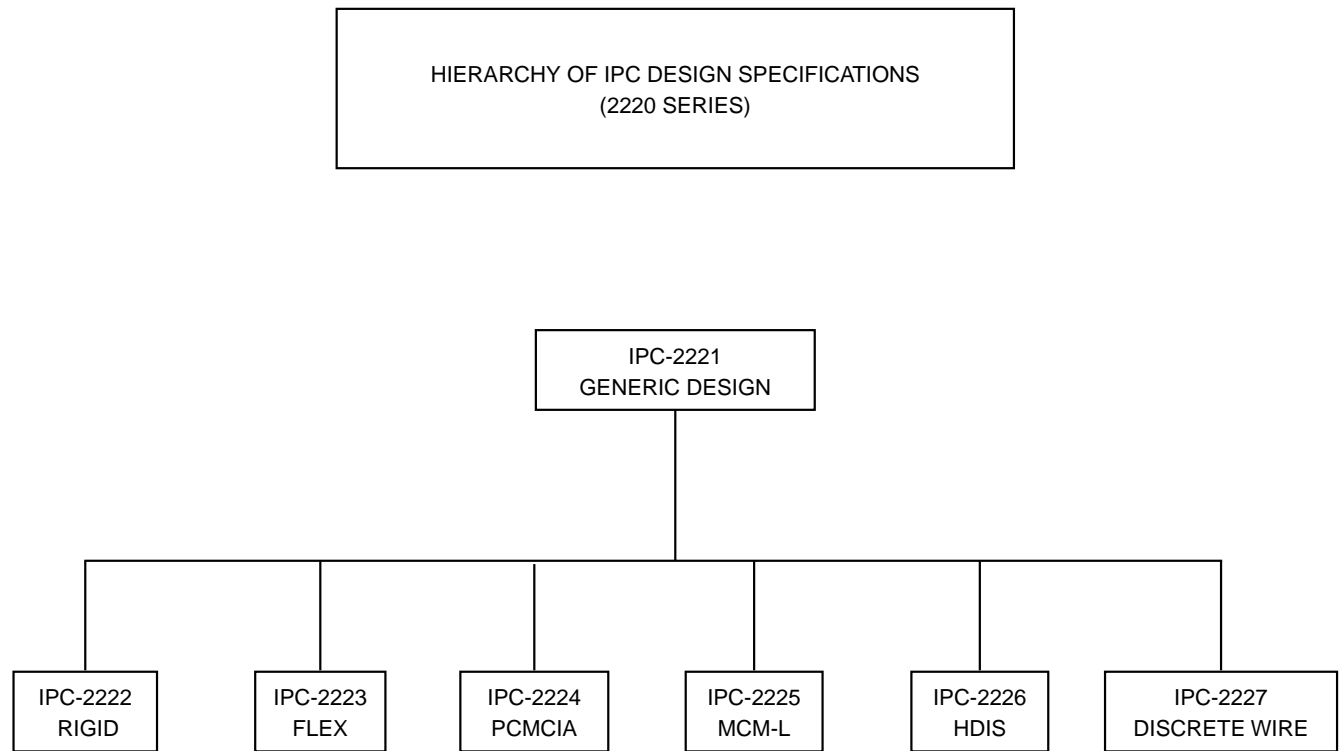
IPC-2225

Sectional Design Standard
for Organic Multichip
Modules (MCM-L) and
MCM-L Assemblies

ANSI/IPC-2225

May 1998

A standard developed by IPC



FOREWORD

This standard is intended to provide information on the detailed requirements for organic Laminated Multichip Module (MCM-L) design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the unique requirements of those designs that use organic rigid (reinforced), organic flexible (unreinforced) materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting unpackaged die.

The information contained herein is intended to supplement generic design requirements identified in IPC-2221. When coupled with the generic design input, it should facilitate the selection process of the materials and the detailed organic structure fabrication technology necessary to meet the engineering design objectives.

The selected component mounting and interconnecting technology for the physical Mounting and Interconnection Structure (MIS) should be commensurate with the requirements provided and the specific focus of this sectional document.

A description of what is an MCM-L and what permutations can be accomplished by mixing other MCM technologies is important to understand to ensure proper design. A detailed description is also provided on the identification of the product in terms of the materials and processes used to manufacture the MCM-L. Other forms of multichip modules are identified in order to establish the relationship with

these technologies (i.e., MCM-C, MCM-D), and the design principles contained herein.

Differences between semiconductors, modules and boards relate to their application and are defined as:

ASIC Application Specific Integrated Circuit represents a semiconductor device intended to satisfy a unique complete circuit function.

ASEA Application Specific Electronic Assembly represents printed board assemblies consisting of electronic components attached to an interconnecting substrate, intended to perform a complete circuit or electronic function.

ASEM Application Specific Electronic Module represents a grouping of components intended as a subassembly or super-part that will be interconnected on an ASEA.

Because of the similarity between various techniques, an attempt to describe the variation between Chip-on-Board (COB) and Multichip Modules (MCM) is described to reflect that:

COB products are ASEAs intended as a complete electronic assembly, using unpackaged chips in whole or in part, which will perform a total electronic function. COB assemblies usually plug into a mother board. For example a PC card can be a COB assembly.

MCM products are ASEMs intended as a super-part or subassembly that will be mounted on an interconnecting structure or substrate.

Table of Contents

1.0 SCOPE	1	4.5.3 Buried Inductors	5
1.1 Purpose.....	1	4.6 Encapsulants, Underfill Materials, and Die Adhesives	5
1.2 Documentation Hierarchy.....	1	4.6.1 Encapsulation Processes	5
1.3 Presentation	1	4.6.2 Underfill (Flip Chip Encapsulation).....	6
1.4 Interpretation	1	4.6.3 Die Attach Materials.....	6
1.5 Classification of Products	1	4.6.4 Solder Resist	6
1.5.1 Assembly Types	1	4.7 Markings and Legends	6
1.5.2 Packaging Density	1	5.0 MECHANICAL/PHYSICAL PROPERTIES	6
1.5.3 Producibility Level	1	6.0 ELECTRICAL PROPERTIES	6
1.6 Terms and Definitions.....	2	7.0 THERMAL MANAGEMENT	6
2.0 APPLICABLE DOCUMENTS	2	7.1 Heat Dissipation Considerations	6
2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)	2	7.2 Comparison with Ceramic.....	7
2.2 Department of Defense.....	3	8.0 COMPONENT AND ASSEMBLY ISSUES	7
2.2.1 Military.....	3	8.1 General Placement Requirements.....	7
2.2.2 Federal.....	3	8.2 Attachment Processes	9
2.3 Other Documents	3	8.2.1 Solder Joining Techniques.....	9
2.3.1 American Society for Testing Materials (ASTM).....	3	8.2.2 Adhesive Interconnection	12
2.3.2 Underwriters Laboratories (UL).....	3	8.2.3 Thermocompression.....	12
3.0 GENERAL REQUIREMENTS	3	8.3 Cleaning	12
3.1 Design Layout.....	3	8.4 Attachment Inspection	12
3.1.1 Design Considerations	3	8.5 Electrical Test.....	13
3.1.2 Density Evaluation.....	3	8.6 Tape Automated Bonding.....	13
3.1.3 Computer Aided Design (CAD) Tools.....	4	9.0 HOLES/INTERCONNECTIONS	13
3.2 Test Requirement Considerations.....	4	9.1 Microvia Fabrication Methods	13
3.2.1 Electrical Test Points	4	9.1.1 Laser Drilling.....	13
4.0 MATERIALS	4	9.1.2 Chemical Drilling	13
4.1 Material Selection.....	4	9.1.3 Photoimaging	13
4.2 Dielectric Base Materials (Including Prepregs and Adhesives).....	4	9.1.4 Punching.....	13
4.2.1 Materials for Sequential Buildup	4	9.1.5 Drilling	13
4.2.2 Materials for Embedded Structure MCM.....	5	9.2 Types of Holes	13
4.2.3 No-flow Prepregs	5	9.2.1 Invisible Via	13
4.3 Laminate Materials	5	9.2.2 Landless Via.....	13
4.4 Conductive Materials.....	5	9.2.3 Land on Via	13
4.4.1 Surface Finishes for Wire Bonding.....	5	9.2.4 Castellated Hole.....	13
4.4.2 Surface Finishes for Die Bonding.....	5	9.2.5 Wrap-Around Via.....	13
4.4.3 Surface Finishes for Flip Chip Attachment	5	10.0 GENERAL CIRCUIT FEATURE REQUIREMENTS	13
4.5 Electronic Component Materials (Buried Resistors and Capacitors)	5	10.1 Conductor Characteristics.....	13
4.5.1 Buried Resistors.....	5	10.1.1 Edge Spacing	15
4.5.2 Buried Capacitors	5	10.1.2 Large Conductive Areas	15

10.1.3	Balanced Conductors	15		
10.2	Land Characteristics	15		
11.0	DOCUMENTATION	15		
11.1	Procurement Documentation Requirements.....	15		
11.2	Multichip Module (MCM-L) Interconnecting Structure.....	15		
11.3	Multichip Module (MCM-L) Construction.....	15		
11.4	Multichip Module (MCM-L) Materials and Specifications	15		
11.5	Hole Formation	15		
11.6	Conductor Definition	15		
11.7	Marking	16		
11.8	Processing Conditions.....	16		
11.9	Special Electrical Performance Requirements.....	16		
11.10	Configuration and Revision Control	16		
11.11	Parts List(s)	16		
11.12	Assembly Drawing	16		
11.13	Electrical Test Requirements	16		
11.14	Schematic/Logic Diagram	16		
11.16	Automated Documentation Package	16		
12.0	QUALITY ASSURANCE	16		
			Figures	
	Figure 4-1	Typical Encapsulation Design Guidelines	6	
	Figure 7-1	Die Attach Using Thermally Conductive Adhesive	8	
	Figure 7-1A	Example of Thermal Via Utilization	8	
	Figure 7-1B	Example of Cavity Structure.....	8	
	Figure 7-1C	Die Bond to Heatsink Plate	9	
	Figure 7-2	Typical Thermal Enhancements for Multilayer Printed Wiring Board Packages	9	
	Figure 7-3	Thermal Characterization of 104-I/O PGA, Chip Facing Down – Ceramic vs. Plastic Multilayer Packages.....	10	
	Figure 7-4	Thermal Characterization of 149-I/O PGA (with Cavity), Facing Down – Ceramic vs. Plastic Multilayer Packages	11	
	Figure 10-1	Etched Conductor Characteristics	14	
			Tables	
	Table 1-1	MCM-L Wiring Capability	1	
	Table 1-2	MCM-L Area (mm ²) for 16 Chips (10 mm x 10 mm)	1	
	Table 3-1	Laminated Multichip Module Interconnect Attributes	4	
	Table 4-1	Microvia Material Properties	5	
	Table 4-2	Encapsulation Technologies for Protection of Bare Die	6	
	Table 4-4	Typical Die Attach Materials	7	
	Table 10-1	Examples of Conductor Widths Tolerances (mm)	15	

Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

1.0 SCOPE

This standard establishes requirements and other considerations (thermal, electrical, electromechanical and mechanical) for the design of organic mounting structure used to interconnect chip components, which in combination form the completed functional Single Chip Module (SCM-L), MCM, or MCM-L assemblies.

1.1 Purpose The purpose of this standard is to establish design principles and recommendations that **shall** be used to produce the appropriate class of multichip module or assembly. Unique design requirements for multichip modules and multichip module assemblies intended for military electronic equipment applications will be noted as such, and **shall** be fabricated by a supplier that has been qualified by the appropriate agency unless otherwise agreed to contractually.

1.2 Documentation Hierarchy Document hierarchy shall be in accordance with generic standard IPC-2221.

1.3 Presentation Presentation shall be in accordance with the generic standard IPC-2221.

1.4 Interpretation Interpretation shall be in accordance with the generic standard IPC-2221.

1.5 Classification of Products Classification of products shall be in accordance with the generic standard IPC-2221 and as follows:

1.5.1 Assembly Types Assembly types are defined as:

Single-sided/Double-sided — Multiple bare and/or chip scale packaged die assemblies analogous to single and double sided printed board assemblies.

Cavity Structures — Multiple bare and/or chip scale packaged die assemblies in which the components are placed into cavities fabricated in the interconnecting structure.

Stacked Structure (includes 3-D memory packages) — Multiple bare and/or chip scale packaged die assemblies in which components are placed one on top of another.

Embedded Structures — Multiple bare and/or chip scale packaged die assemblies in which components are embedded within the interconnecting structure requiring lamination over bare die and subsequently interconnected.

Multi-Mounting Structure — Combination of any above assembly types.

1.5.2 Packaging Density The assembly of uncased or bare chips on substrates has become popular mostly due to the ability of such assemblies to reduce the area needed for interconnecting substrates. The ideal limit for such assembly would be to place all the chips tightly together, without any space in between. This would result in 100% of Packaging Efficiency, a ratio of silicon area to the substrate area. Naturally, 100% efficiency is not achievable, but this ratio is still useful in ranking various substrate construction of bare chip attachment methods.

Table 1-1 shows the different feature resolution capabilities, i.e., line widths and spacings, for the MCM-L mounting structure construction and their respective wiring density capability.

Table 1-1 MCM-L Wiring Capability

Typical wiring capability cm/cm ² layer	Typical signal plane	Total wiring capability cm/cm ²
Standard 15	4S 8S	60 30
Extended 25	4S 8S	100 200
Sequential 30-50	2S 4S	60/100 120/200

Table 1-2 tabulates the total substrate area needed to place 16 chips (10 mm x 10 mm) on a MCM-L mounting structure using four typical chip wiring methods.

Table 1-2 MCM-L Area (mm²) for 16 Chips (10 mm x 10 mm)

	Flip Chip	Wire Bond	Flip TAB	Reg TAB
MCM-L S/S	2500	6200	7000	8400
MCM-L D/S	1800	4300	4900	5900

1.5.3 Producibility Level Although multichip modules are usually high density interconnecting structures of bare chips, there are times when only a few bare chips are necessary to accomplish the goal of the multichip module designer. In these instances interconnection area relates to the amount of area of silicon die occupied on the module. Thus a general approximation has been made in the three levels as to the percentage of silicon area occupied on the interconnecting substrate.

The three MCM levels and their associated silicon area densities are:

Level A General Design Complexity—Preferred (<40% area density)

Level B Moderate Design Complexity—Standard (40 - 70% area density)

Level C High Design Complexity—Reduced (>70% area density)

1.6 Terms and Definitions The definition of terms used herein **shall** be as specified in IPC-T-50 or as listed below:

Organic Multichip Module (MCM-L) — A packaged assembly of unpackaged or minimally-packaged components mounted on an interconnecting structure or substrate which is fabricated using primarily printed board manufacturing processes and organic materials.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this standard to the extent specified herein. The revision of the document in effect at the time of solicitation **shall** take precedence.

2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CC-110 Guidelines for Selecting Core Constructions for Multilayer Printed Wiring Board Applications

IPC-L-125 Specification for Plastic Substrates, Clad or Unclad, for High Speed/High Frequency Interconnections

IPC-MF-150 Metal Foil for Printed Wiring Applications

IPC-CF-152 Composite Metallic Materials Specification for Printed Wiring Boards

IPC-FC-232 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-310 Guidelines for Phototool Generation and Measurement Techniques

IPC-D-317 Design Guidelines for Electronic Packaging Utilizing High-speed Techniques

IPC-D-325 Documentation Requirements for Printed Boards, Assemblies, and Support Drawings

IPC-D-350 Printed Board Description in Digital Form

IPC-AM-372 Electroless Copper Film for Additive Printed Boards

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual

Method 2.1.1 Microsectioning

Method 2.1.6 Thickness, Glass Fabric

Method 2.6.3 Moisture and Insulation Resistance, Rigid, Rigid/Flex and Flex/Printed Wiring Boards

IPC-ET-652 Guidelines for Electrical Testing of Printed Wiring Boards

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-SM-786 Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-2221 Generic Standard on Organic Printed Board Design

IPC-2510 Series

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

IPC-2513 Drawing Methods for Manufacturing Data Description

IPC-2514 Printed Board Manufacturing Data Description

IPC-2515 Bare Board Product Electrical Testing Data Description

IPC-2516 Assembled Board Product Manufacturing Data Description

IPC-2518 Parts List Product Data Description

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4101 Laminate/Prepreg Materials Standard for Printed Boards

IPC-6015 Performance Requirements for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

1. Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062.