ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

IPC-2221

Generic Standard on Printed Board Design

Amendment 1

IPC-2221

A standard developed by IPC

Amendment 1
January 2000

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- Minimize time to market
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Para 1.6.3 Title **"Producibility Level"** should be **"Complexity Level."**

Para 4.2.3 First paragraph, first sentence: Replace reference to MIL-S-13949 with IPC-4101.

Para 4.4 Add fifth sentence: ''Attention should be paid to the effects of dissimilar metals in areas such as: connectors, sockets, and other interfaces. The result of a poor material selection could be a reduction in function, either mechanical or electrical.''

Para 4.5.1 Append following the third paragraph:

If the application or design mandates, the minimum and/or maximum solder mask thickness **shall** be specified on the Master Drawing. The minimum thickness specification is required to meet insulation resistance requirements and **shall** be calculated from SM material specifications. The maximum thickness specification is required for component assembly process issues, such as solder paste applications.

Para 4.5.2.1 Second paragraph, second sentence, replace ''jeopardize are circuits'' with ''jeopardize bare circuits.''

Para 5.3.2 First paragraph, second sentence, replace reference to paragraph 8.1.12 with reference to paragraph 8.1.9.

Para 5.4.3 Section C. Fifth sentence should read: ''...with respect to the assembly tooling holes (see Figure 5-6).''

Para 6.2 First paragraph, second sentence. Add following end of sentence:

$$I = k\Delta T^{0.44} A^{0.725}$$

Where I = current in amperes, A = cross section in sq. mils, and ΔT = temperature rise in °C

Para 6.4.1 Variable c, change ''(3.0x108 m/s)'' to : 3.0 X 10^8 m/s.

Table 6-2 Change ''MIL-S-13949'' to ''IPC-4101.''

Para 7.1.2 Fourth paragraph, second sentence, change ''principle'' to ''principal.''

Figure 7-1 Should be dimensioned in Imperial Units.

Para 8.3.1.6 First paragraph, first sentence: Replace reference to para 8.1.14 with para 8.1.11.

Para 9.1.1 Variable *a*, add: Note: For external layers, the requirement is the maximum diameter of the finished hole. For internal layers, the drilled hole diameter is used.

Para 9.1.1 Variable *b*, add: Note. Etchback must be included within the calculation.*

Para 9.2.7.1 First paragraph, last sentence: Replace ''solder form'' with ''solder from.''

Para 10.1.1 Third paragraph, second sentence should read: ''The nominal finished conductor width and acceptable tolerances, **shall** be shown on the master drawing.''

Replace Para 12.4.1 as follows:

12.4.1 Specimen A and B (Plated Hole Evaluation) Test specimen A and B are used to evaluate plated hole characteristics. Test specimen A is used for solderability and rework simulation containing the largest component hole and land associated with that hole that can be fitted on a 2.5 mm [0.0984 in] grid. Test specimen B is used for thermal stress testing and contains the smallest through hole on the board and its associated land. This is the hole which is the most difficult to plate and is exposed to the greatest Z axis stress. When outer layer interconnecting blind holes exist, a minimum of one additional B specimen **shall** be added to represent the most complex blind hole.

For thermal stress testing, when there is a combination of both via and component holes on the same pcb, the following is mandated: Either the B coupon **shall** reflect both hole sizes, or both A&B **shall** be used for sampling purposes. For this purpose, the B coupon **shall** be designed so as to provide a minimum of three holes of each size.

Figure 12-2 shows the general configuration of the specimen. The land shape **shall** be the same as that used on the printed board for these lands and holes. Imaged layers **shall** represent printed board design, e.g., ground ties on specific layers, deleted non-functional lands, etc.

For internal layers connection holes (blind and buried vias) a minimum of one additional B specimen **shall** be added for each interconnection plating operation required by the design. See Figure 12-3 for an example of additional B coupon use.

Note: Coupon S may be substituted for solderability testing (see 12.4.9 and Figure 12-18. Specimen A is not required for non-through hold SMT designs (see 12.4.7 and Figure 12-6).

Para 12.4.9 Fourth sentence, replace with ''this specimen is referenced in J-STD-003.''

Add new Para 12.4.12 Specimen X This specimen **shall** be used to validate bending flexibility and bending endurance of flexible printed wiring applications. This specimen is typically used for qualification and/or acceptance testing of flexible products designed for installation use B (dynamic flex). The specimen should represent the circuit conductor characteristics of the actual design. The outline of the specimen as shown in Figure 12-20 **shall not** be deviated from in order to accommodate the test method fixture. The number of minimum flex life cycles should be specified on the master drawing. Refer to IPC-2223 for specific design flexibility guidelines.

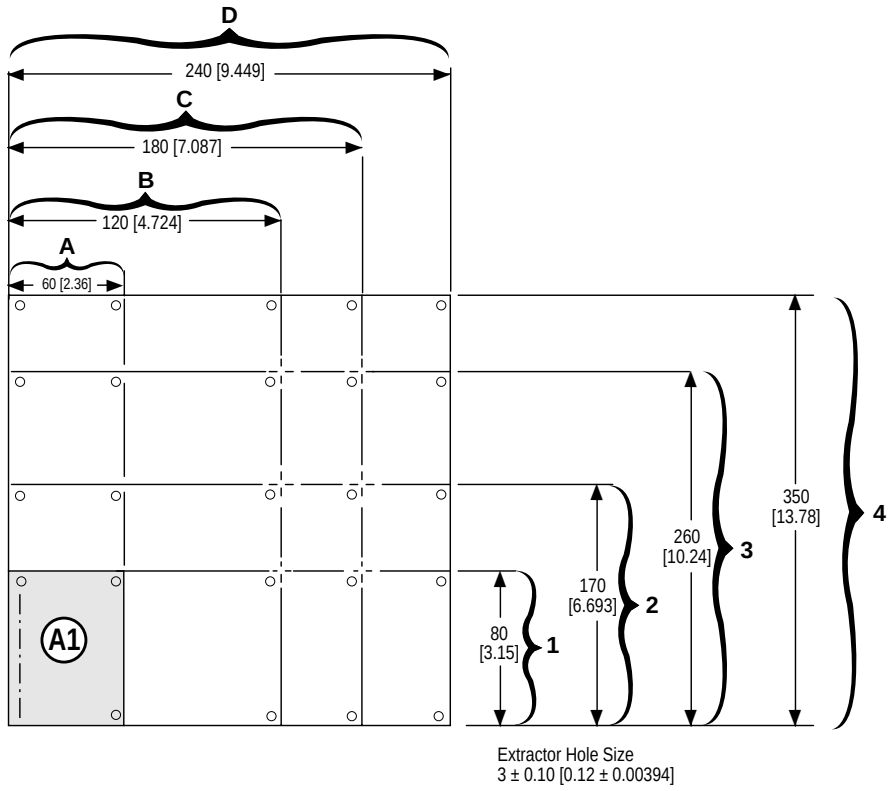
Appendix A First column, last bullet should read: ''Avoid ''wired'OR'' and ''wired'AND'' connections. If you cannot, use gates from the same integrated circuit package.''

Appendix A Second column, first bullet: Delete.

Appendix A Second column, sixteenth bullet should read ''...complex circuit lines to an integrated circuit package.''

Replace Figure 5-1 as follows:

Board No.	Printed Board Size ± 0.4 [0.016]
A1	80 x 60 [3.15 x 2.36]
A2	80 x 120 [3.15 x 4.724]
A3	80 x 180 [3.15 x 7.087]
A4	80 x 240 [3.15 x 0.449]
B1	170 x 60 [6.693 x 2.36]
B2	170 x 120 [6.693 x 4.724]
B3	170 x 180 [6.693 x 7.087]
B4	170 x 240 [6.693 x 9.449]
C1	260 x 60 [10.24 x 2.36]
C2	260 x 120 [10.24 x 4.724]
C3	260 x 180 [10.24 x 7.087]
C4	260 x 240 [10.24 x 9.449]
D1	350 x 60 [13.78 x 2.36]
D2	350 x 120 [13.78 x 4.724]
D3	350 x 180 [13.78 x 7.087]
D4	350 x 240 [13.78 x 9.449] [Not recommended for Best Panel Utilization]



IPC-2221-5-1

Figure 5-1 Example of printed board size standardization, mm [in]

Replace Figure 5-7 as follows:

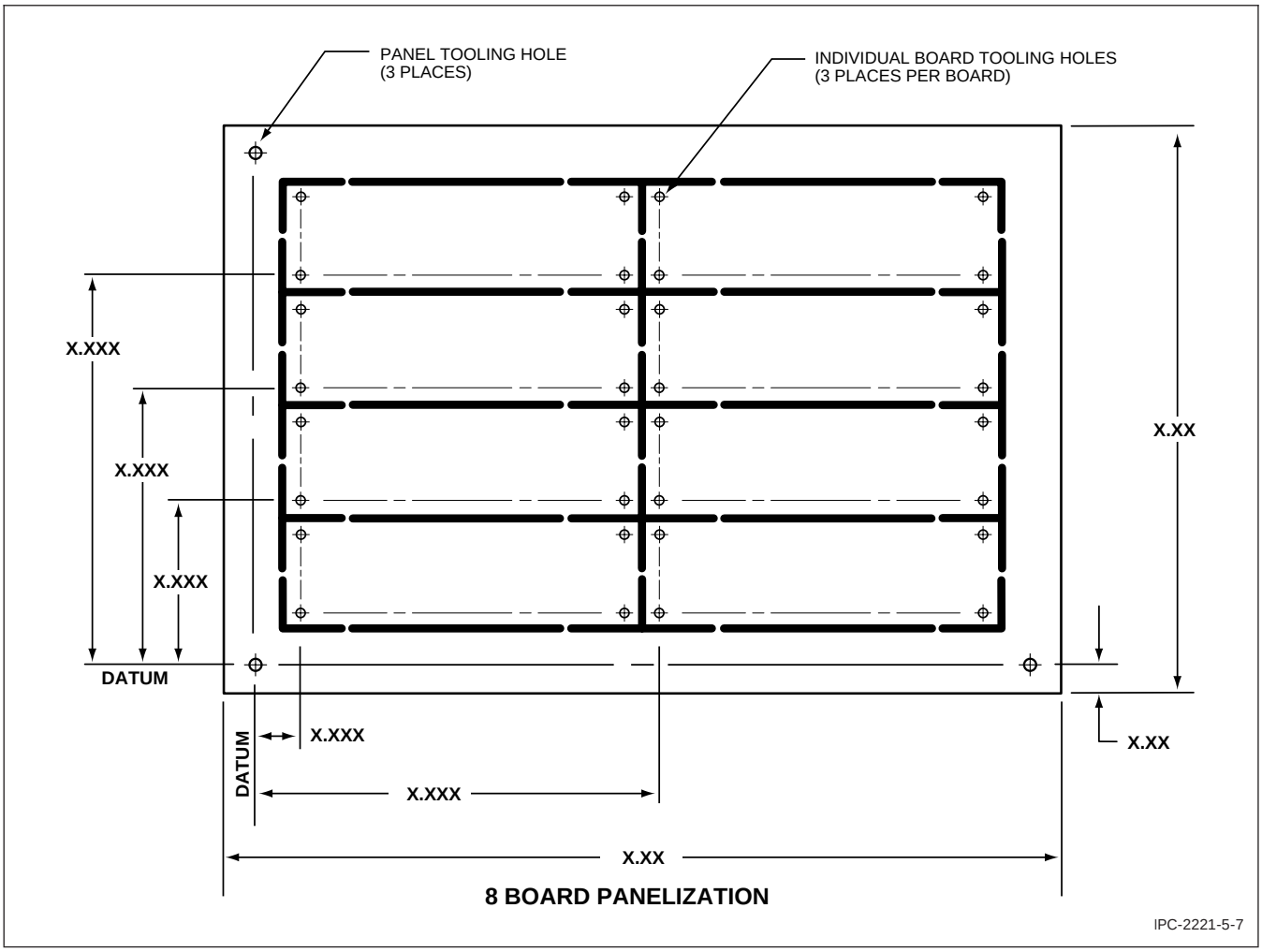


Figure 5-7 Datum Features for Panelization

Replace Figure 6-7 as follows:

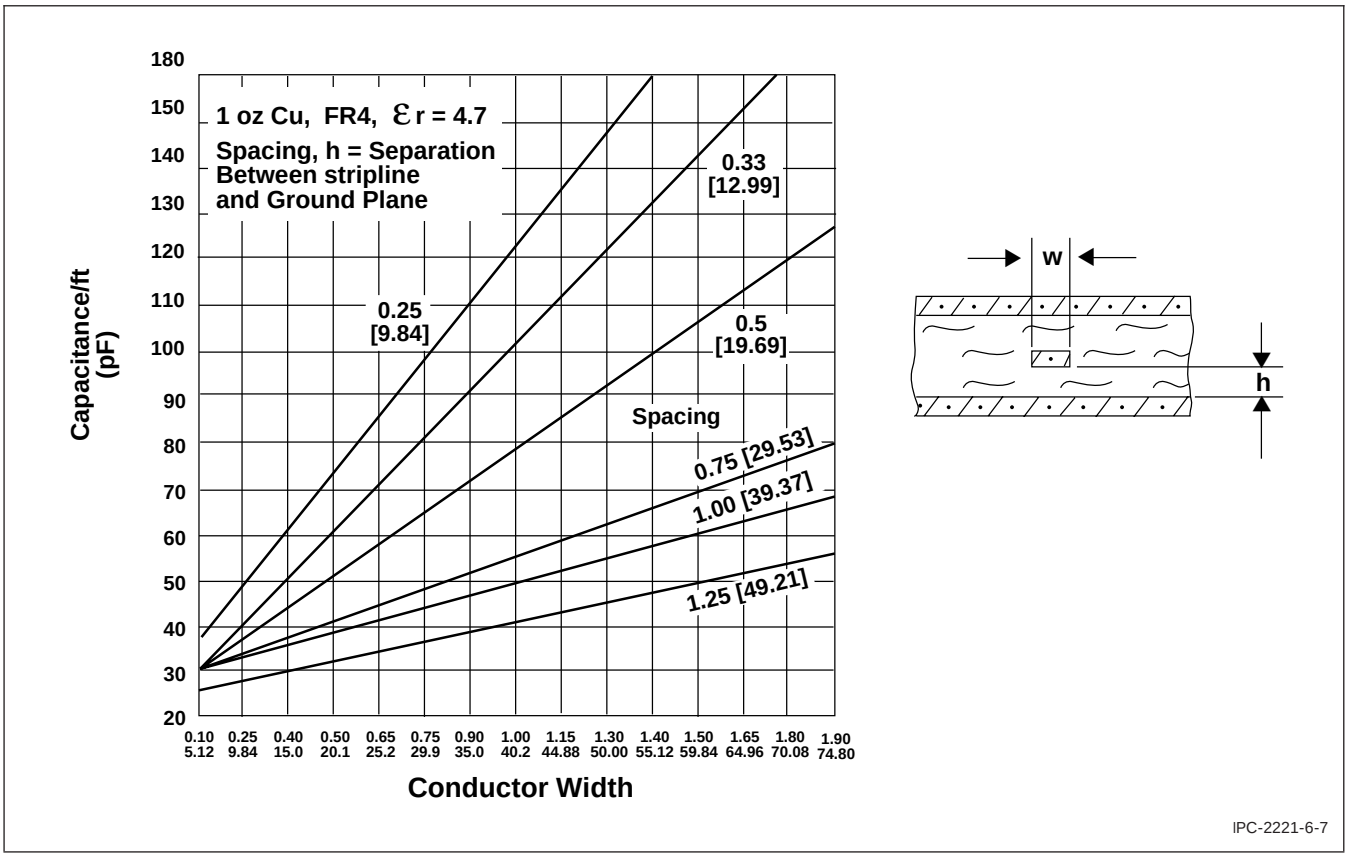


Figure 6-7 Capacitance vs. conductor width and spacing for striplines, mm [mils]

Replace Figure 8-16 as follows:

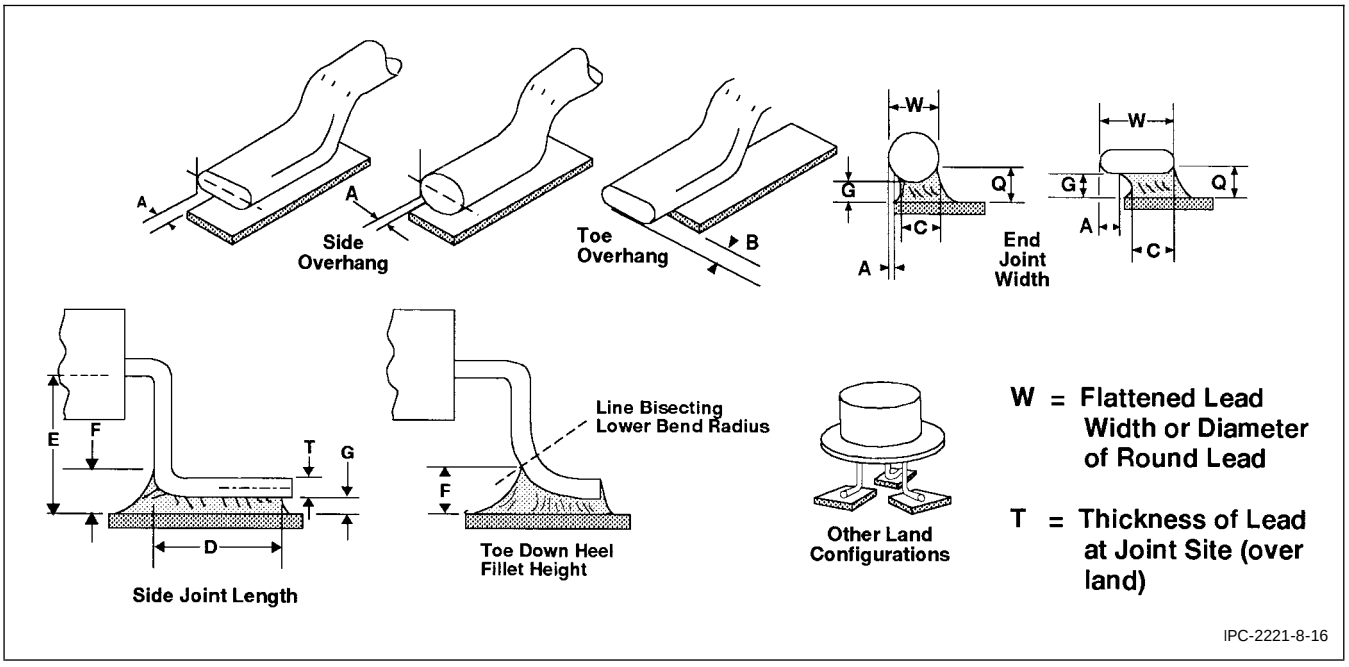


Figure 8-16 Round or flattened (coined) lead joint description

Replace Figure 8-25 as follows:

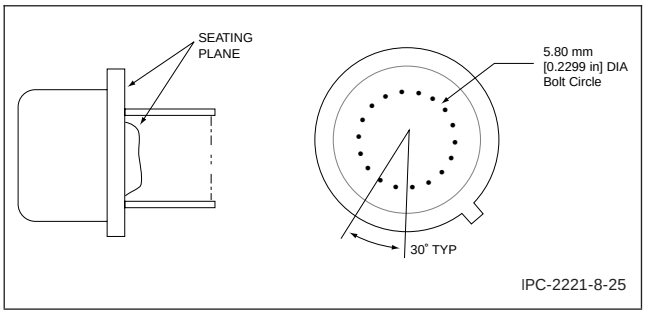


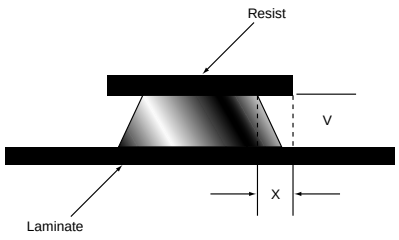
Figure 8-25 "TO" can radial-leaded component, mm [in]

Replace Table 9-2 as follows:

Table 9-2 Annular Rings (Minimum)

Annular Ring	Class 1, 2, and 3
Internal Supported	0.025 mm [0.000984 in]
External Supported	0.050 mm [0.00197 in]
External Unsupported	0.150 mm [0.005906 in]

Replace Figure 10-3 as follows:



$$\text{Etch Factor} = \frac{V}{X}$$

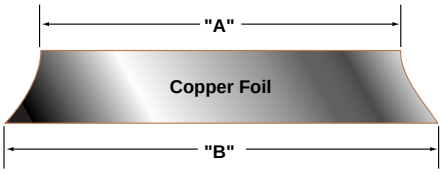
"A" POINT OF NARROWEST CONDUCTOR WIDTH: This is not "Minimum Conductor Width" noted on master drawings or performance specifications.

"B" CONDUCTOR BASE WIDTH: The width that is measured when "Minimum Conductor Width" is noted on the master drawing or performance specification.

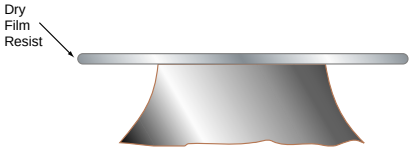
"C" PRODUCTION MASTER WIDTH: The width usually determines the width of the metal or organic resist on the etched conductor.

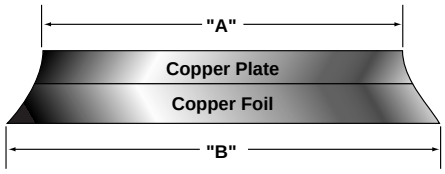
Design width of the conductor is specified on the master drawing and is most often measured at the conductor base "B" for compliance to "minimum conductor width" requirements.

The following two configurations show that conductor width may be greater at the surface than at the base.

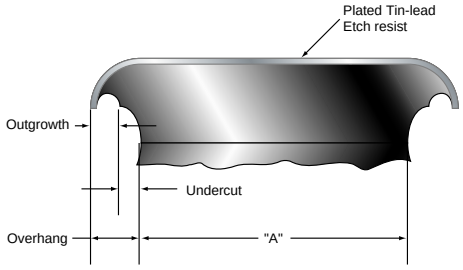


Internal layer after etch

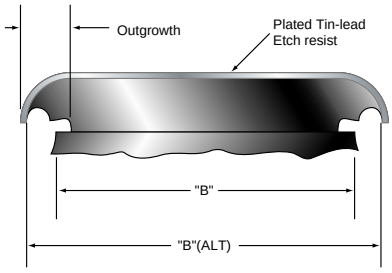




Internal plated layer as used for buried vias



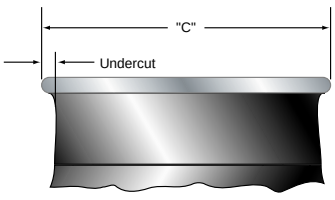
Pattern plating (dry film resist) with outgrowth



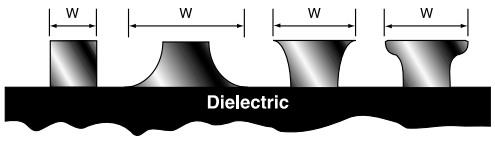
Pattern plating (liquid resist) with outgrowth

Note: The extent of outgrowth, if present, is related to the dry film resist thickness. Outgrowth occurs when the plating thickness exceeds the resist thickness.

"B" (ALT) would be used to determine compliance with "Minimum Conductor Width" for this etch configuration.



Thin clad & pattern plating (etch resist)



The effective width of a conductor may vary from the conductor width from surface obstructions (W).

Note: The different etch configurations may not meet intended design requirements.

IPC-2221-10-3

Figure 10-3 Etched Conductor Characteristics

Replace Table 12-1 as follows:

Table 12-1 Specimen Frequency Requirements[1]

Specimen Purpose	I.D.[2]	Class 1	Class 2	Class 3
Conformance Testing				
Hole Solderability, Rework Simulation	A	Not required	Twice per panel	Twice per panel, opposite corners
Solderability	S	Optional	Optional	Optional
Solder Resist Tenting (if used)	T	Not required	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Thermal Stress, Plating Thickness, and Bond Strength Type 1	B	Twice per panel opposite corners	Twice per panel opposite corners	Twice per panel opposite corners
Plating Adhesion and Surface Solderability	C	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel location optional, pattern defined by artwork
Solder Resist (if used)	G	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Surface Mount Solderability (Optional for SMT)	M	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Reliability Assurance Inspection				
Surface Mount Bond Strength (Optional for SMT)	N	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Surface Insulation Resistance	H	Once per panel, location optional	Twice per panel opposite corners	Twice per panel opposite corners
Moisture and Insulation Resistance	E	Once per panel, location optional	Twice per panel, opposite corners	Twice per panel opposite corners
Optional or Process Control				
Registration (Option 1 or 2)	F	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Registration (Optional)	R	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Interconnect Resistance (Optional 1 or 2)	D	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Bending Flexibility, Flexible Endurance	X	Optional, pattern defined by artwork	Optional, pattern defined by artwork	Optional, pattern defined by artwork

[1] If additional coupons for impedance testing are required, follow guidelines of IPC-D-317 and IPC-2141.

[2] Where possible, coupon identification letters have been chosen to conform to those currently being used for conformance evaluations.

Replace Figure 12-2 as follows:

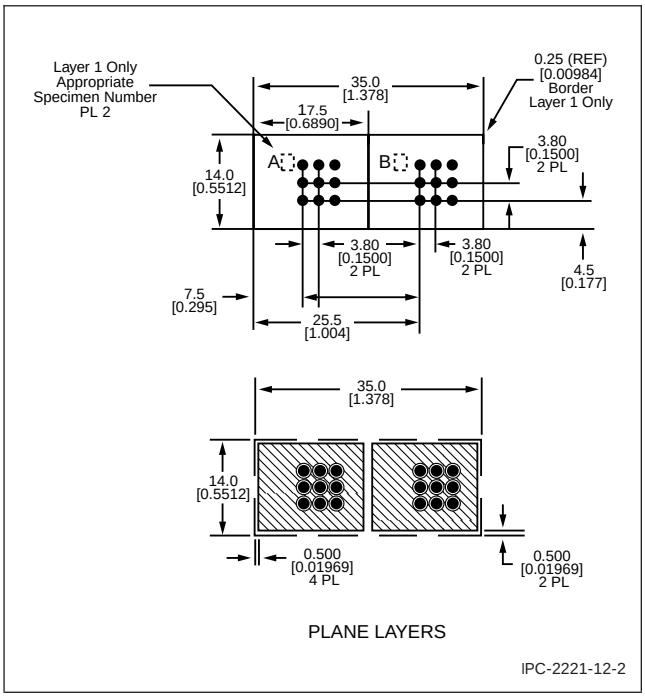


Figure 12-2 Test Specimen A and B, mm [in]

Figure 12-3, replace with new Figure 12-3 as follows:

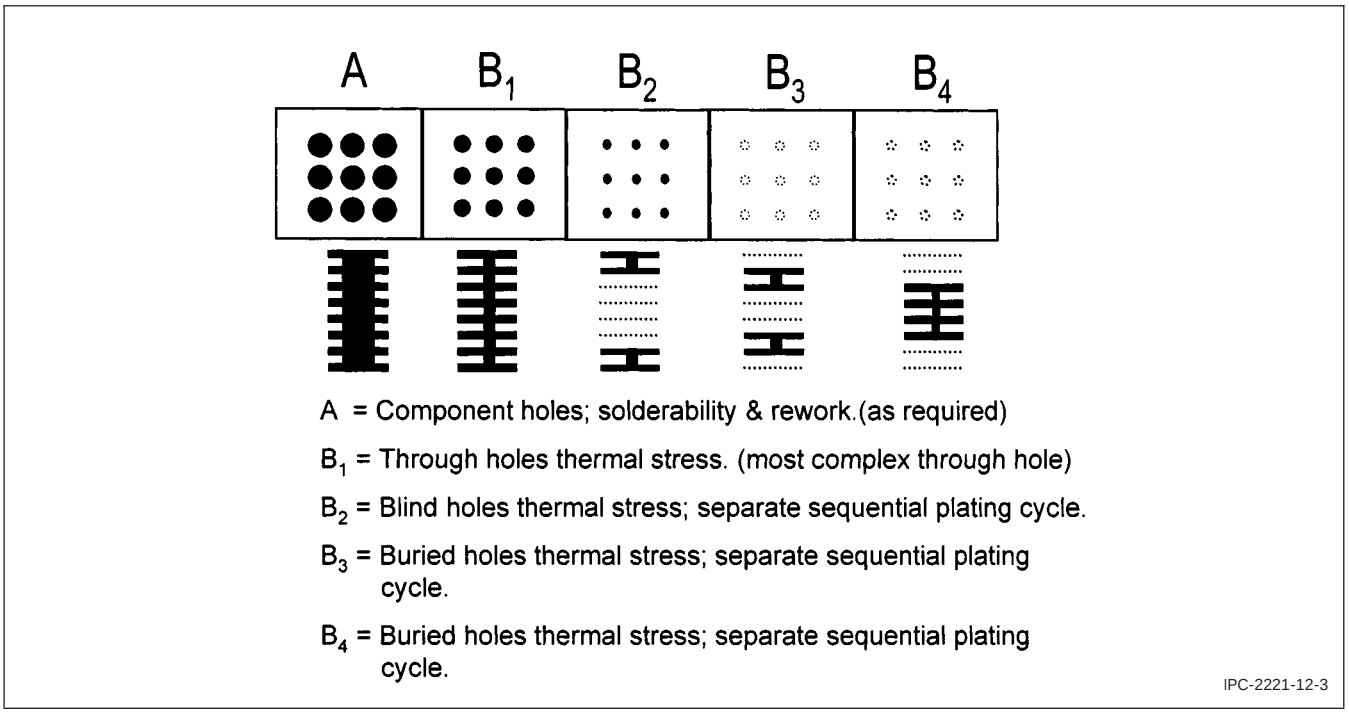


Figure 12-3 Test Specimen A and B (example of multiple coupon use for an IPC-6012 Type 4 PWB design)

Figure 12-18, Test Specimen S, replace as follows:

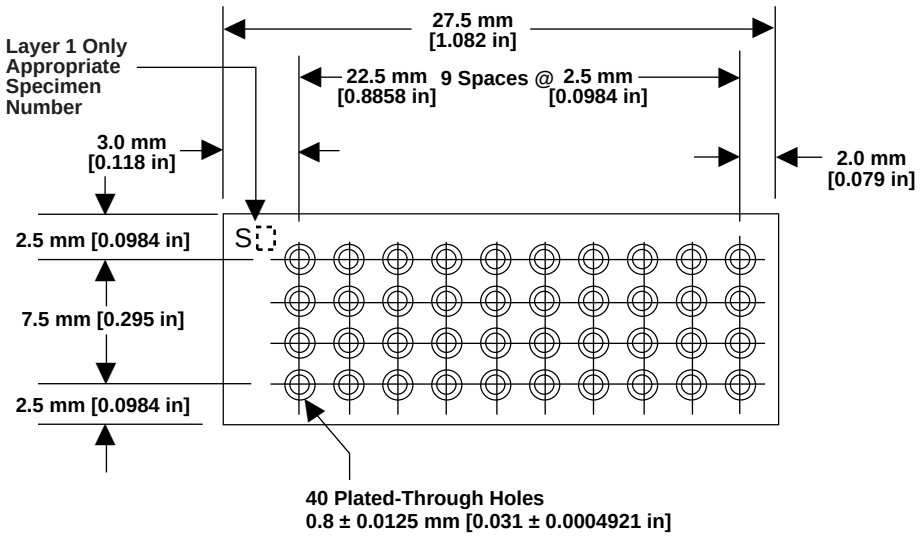


Figure 12-18 Suggested Test Specimen for Plated-Through Holes

Insert Figure 12-20 as follows:

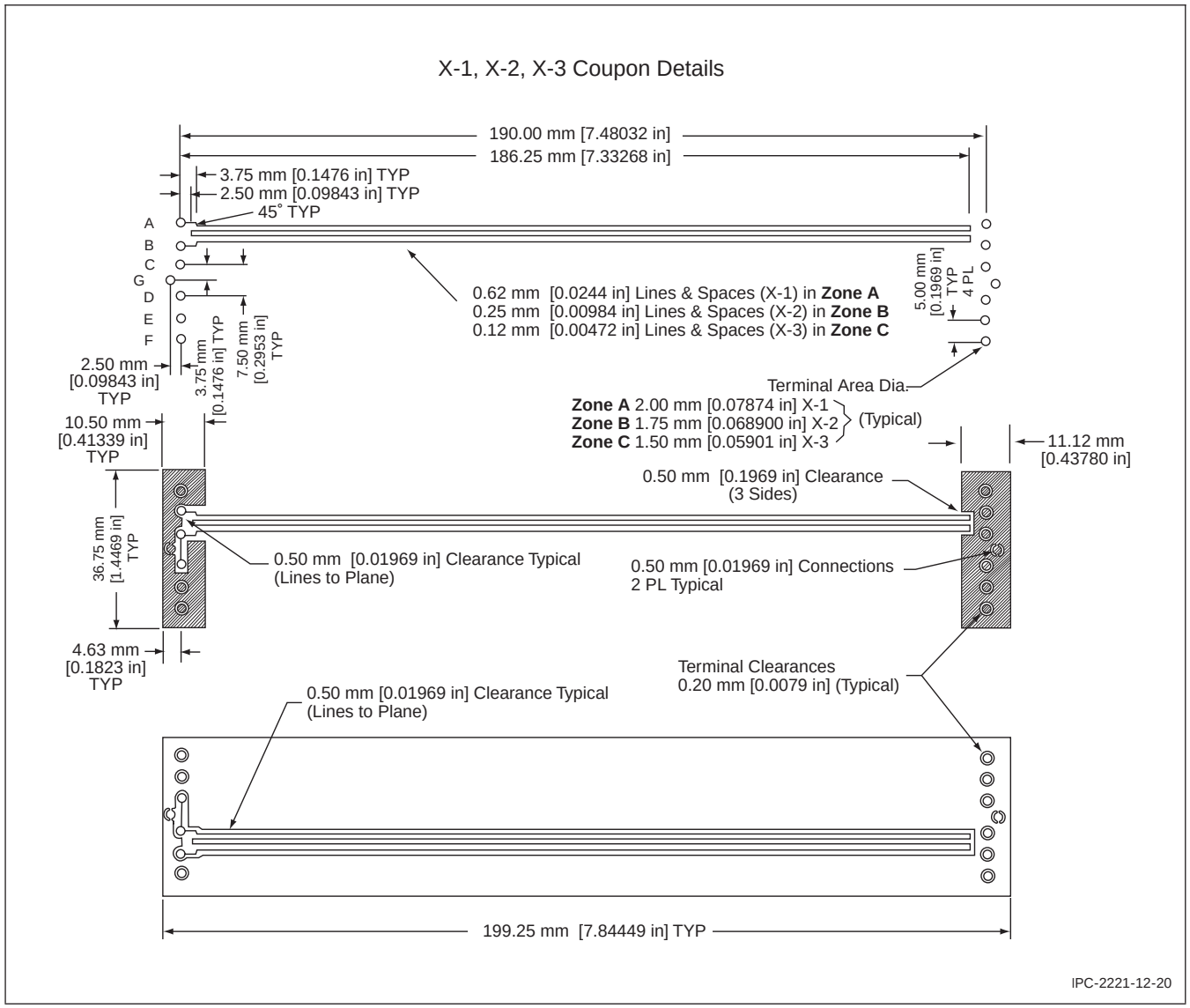


Figure 12-20 Test Specimen X, mm [in]

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ISBN #1-580982-36-0

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