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Controlled Impedance Circuit Boards and High Speed Logic Design

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Table of Contents

1.0 Scope 1
2.0 References 1
3.0 Engineering Design Overview 1
3.1 Device Selection 1
3.2 Intraconnection 2
3.2.1 Connectors 2
3.2.2 Cables 2
3.3 Printed Board and Printed Board Assemblies 2
3.3.1 Board Design 2
3.4 Performance Requirements 3
3.4.1 Power Distribution 3
3.4.2 Relative Permittivity (Dielectric Constant) 3
3.4.3 Relative Permittivity and Frequency Relationship 4
3.4.4 Critical Signal Speed 4
3.4.5 Capacitive Line Versus Controlled Impedance Line Environment 5
3.4.5.1 Capacitive Line 5
3.4.5.2 Controlled Impedance Line 5
3.4.6 Bandwidth 6
3.4.7 Propagation Time 6
3.4.7.1 Propagation Delay Time 6
3.4.8 Signal Loading Effects 6
3.4.9 Crosstalk 7
3.4.10 Signal Attenuation 7
3.4.11 Termination of Nets 8
3.4.12 Additional Signal Integrity Issues 8
3.4.12.1 Skew 8
3.4.12.2 Reflections 8
3.4.12.3 Ring Back 8
3.4.12.4 Threshold 8
3.4.12.5 V_{cc}/Ground Bounce 8
3.4.13 Switching Noise 10
3.4.14 Other Parasitics Noise 10
3.4.15 Noise Budget/Noise Margin 10
3.5 Power Distribution 10
3.5.1 DC Power Distribution 10
3.5.2 AC power Distribution 10
4.0 Design of Controlled Impedance Circuits 11
4.1 Unbalanced Line Configurations 11
4.2 Unbalanced Line Equations 11
4.2.1 Surface Microstrip, Figure 4c 12
4.2.2 Embedded Microstrip, Figure 4d 12
4.2.3 Symmetric Stripline, Figure 4e 12
4.2.4 Dual (Asymmetric) Stripline, Figure 4f 12
4.2.5 Wire Stripline, Figure 4a 13
4.2.6 Wire Microstrip, Figure 4b 13
4.3 Balanced Line Configuration 13
4.4 Balanced Line Equations 14
4.4.1 Surface Microstrip 14
4.4.2 Embedded Microstrip 14
4.4.3 Symmetric Stripline 14
4.5 Controlled Impedance Design Rules 14
4.6 Crosstalk Rules 16
4.6.1 Crosstalk Implementation 16
4.7 Controlled Impedance Coupon Design Rules 16
4.8 Decoupling/Capacitor Rules 16
4.8.1 Decoupling Capacitance 16
4.8.2 Transient Capacitance Consideration 17
4.8.3 Line Charging Capacitance 17
4.8.4 Low Frequency (Bulk) Capacitance 18
4.8.5 Capacitor Model 18
4.8.6 Decoupling/Capacitor Design Rules 18
5.0 Design For Manufacturing 19
5.1 Process Rules in CAD 19
5.2 Design Complexity and Correlation to Cost 19
6.0 Data Description 19
6.1 Details of Construction 19
6.1.1 Controlled Construction 19
6.1.2 Controlled Performance - Controlled Capacitance or Controlled Impedance 19
6.2 Isolation of Data by Net Class (Noise, Timing, Capacitance, and Impedance) 19
6.3 Electrical Performance 20
7.0 Material 20
7.1 Resin Systems 20
7.2 Reinforcements 20
7.3 Prepregs, Bonding Layers and Adhesives 20
7.4 Frequency Dependence 20
8.0 Fabrication 20
8.1 General 21
8.2 Preproduction Processes 21
8.2.1 Artwork Verification 21
8.2.1.1 Electronic Data 21
8.2.1.2 Phototools 21

8.2.2 Panelization ... 21
8.2.3 Tooling ... 21
8.2.4 Plotting ... 21
8.2.5 Artwork Inspection ... 21
8.3 Production Processes ... 22
8.3.1 Processing Considerations ... 22
8.3.2 Laminate, Expose & Develop Cores ... 22
8.3.3 Innerlayer Etching ... 22
8.3.4 Scan (AOI) ... 22
8.3.5 Lamination ... 22
8.3.6 Hole Formation ... 22
8.3.7 Photo Expose and Develop ... 23
8.3.8 Electrolytic (Pattern) Plate ... 24
8.3.9 Outer Layer Strip, Etch ... 24
8.3.10 Solder Mask ... 24
8.4 Impact of Defects at High Frequencies ... 24
8.4.1 Copper ... 24
8.4.1.1 General ... 24
8.4.1.2 Conductor Cross-Section ... 24
8.4.1.3 Pin-Holes ... 24
8.4.1.4 Spurious Copper ... 24
8.4.1.5 Copper Thickness ... 24
8.4.1.6 Surface Preparations ... 24
8.4.2 Substrate ... 24
8.4.2.1 General ... 24
8.4.2.2 Dielectric Constant (Relative Permittivity) ... 24
8.4.2.3 Loss Tangent ... 25
8.4.2.4 Laminate Consistency ... 25
8.4.2.5 Prepreg ... 25
8.4.2.6 Inclusions ... 25
8.4.2.7 Voids ... 25
8.4.2.8 Resin Flow and Content ... 25
8.5 Data Description ... 25
8.5.1 Type of CAD Data ... 25
8.5.2 Customer Interface ... 25

9.0 Time Domain Reflectometry Testing ... 25
9.1 TDR Method of Choice ... 25
9.1.1 Standard Test Coupon ... 25
9.1.2 Types Of Test Specimen ... 25
9.2 Equipment ... 26
9.2.1 Time Domain Reflectometry Method ... 26
9.2.1.1 Method for Consistent TDR Testing ... 26
9.2.1.2 Test Equipment Specification ... 26
9.2.1.3 Rise Time & Bandwidth Requirement ... 26
9.2.1.4 Step Flatness ... 27
9.2.1.5 Other Parameters ... 27
9.2.1.6 Protection ... 27
9.2.1.7 Test Procedure ... 27
9.2.1.8 Differential Test ... 27
9.2.2 Calibration Techniques ... 29
9.2.2.1 Cables ... 29
9.2.2.2 Reference Impedance ... 29
9.2.3 Standard Test Probe and Fixture ... 29
9.2.3.1 Connectors ... 29
9.2.3.2 Probes ... 29
9.2.3.3 Fixturing ... 30
9.2.4 Correlation of Equipment Types and Laboratories ... 30
9.2.4.1 Correlation Of Different Equipment Types ... 30
9.3 Training ... 30
9.3.1 Operator Skill Level ... 30
9.3.2 Operator Knowledge ... 31

Appendix A Units, Symbols, and Terminology ... 32

Appendix B Bibliography ... 33

Figures

Figure 1 Switching Speed vs Propagation Delay ... 3
Figure 2 ε_r Versus Frequency (FR4) ... 5
Figure 3 Termination of Nets ... 9
Figure 4 Typical Unbalanced Line Configurations ... 12
Figure 5 Unbalanced Line Schematic ... 13
Figure 6 Unbalanced Line Circuit Boards ... 13
Figure 7 Balanced Line Diagram ... 13
Figure 8 Balanced Line Circuit Board ... 14
Figure 9 Typical Balanced Line Configuration ... 15
Figure 10 Impedance Control Test Coupon ... 17
Figure 11 Test Probe Patterns ... 18
Figure 12 Flow Chart of Pre-production Processes ... 22
Figure 13 Production Process Flow Chart ... 23
Figure 14 Typical TDR Test Set Up, Unbalanced Line ... 28
Figure 15 TDR Waveform ... 28
Figure 16 Typical TDR Test Set Up, Balanced Line ... 28
Figure 17 Typical Single Ended Unbalanced TDR Test Setup ... 29
Figure 18 Typical Differential Balanced TDR Test Setup ... 30
Figure 19 Typical PC Controller TDR Waveform Display ... 31

Tables

Table 1 Device Rise Time ... 5
Table 2 Typical data for some logic families ... 7
Table 3 Propagation time in various materials ... 7

Controlled Impedance Circuit Boards and High Speed Logic Design

1.0 Scope

This guide is intended to be used by circuit designers, packaging engineers, printed board fabricators, and procurement personnel so that all may have a common understanding of each area.

The goal in packaging is to transfer a signal from one device to one or more other devices, through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique consideration.

2.0 References

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

IPC T-50 Terms and Definitions for Printed Circuits

IPC-L-108 Specification for Thin Laminates, Metal Clad Primarily for High Temperature Multilayer Printed Boards

IPC-L-109 Specification for Glass Cloth, Resin Preimpregnated (B-Stage) for High Temperature Multilayer Printed Boards

IPC-L-115 Specification for Plastic Sheet, Laminated Metal Clad for High Temperature Performance Printed Boards

IPC-TM-650 Test Methods Manual
T.M. 2.5.5.7 Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR[1]

IPC-D-317 Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

IPC-2220 Design of Organic Printed Boards and Printed Board Assemblies

The references presented in the bibliography may provide more comprehensive treatment of the subject.

3.0 Engineering Design Overview

Packaging of electronic equipment has traditionally been an area for mechanical considerations. Packaging design is becoming more complex as today's electronics technologies are available in greater switching speed and higher density per chip. Individual chips have greater numbers of connections in smaller chip package sizes. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. Controlled impedance circuit boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor with interconnections specified in to/from wire listing or net lists. Electrical conductor signals were routed with only a few concerns, that continuity was maintained between points, conductors had sufficient copper for the current and clearance was maintained to prevent voltage breakdown. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits have introduced new devices with extremely fast rise times which are housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

With recent advances in semiconductor processing technology, CMOS outputs have output impedance approaching the ECL (5-6 ohms) and can switch 50 ohm lines in as little as 1 nonosecond from one logic level to the other, a swing of 5 volts. These fast edges demand all of the concern normally given the GaAs and ECL logic families.

3.1 Device Selection

Device technology options include TTL, Schottky TTL, CMOS, ECL and GaAs, each with its own set of power requirements, operating temperature range, density of chip, input impedance, output impedance, signal threshold levels, noise sensitivity, response time and output pulse rise/fall time. Many designs will have mixed technology where SMT and through-hole packaging is intermixed with TTL, CMOS and ECL logic that may require multiple line widths (impedance values) on the same circuit layer or may compromise on a single conductor width that can provide enough margin for the different logic families.

1. The test method has been included for convenience.